0.5 Ω 1.8V to 5.5V CMOS Dual DPDT in WLCSP/LFCSP Package

Preliminary Technical Data

ADG888

FEATURES

+1.8 V to +5.5 V operation
Ultra-Low On resistance:
- **0.5 Ω typical**
- **0.8 Ω max at 5V supply**

Excellent audio performance, ultralow Distortion:
- **0.01 Ω typical**
- **0.2 Ω max Ron flatness**

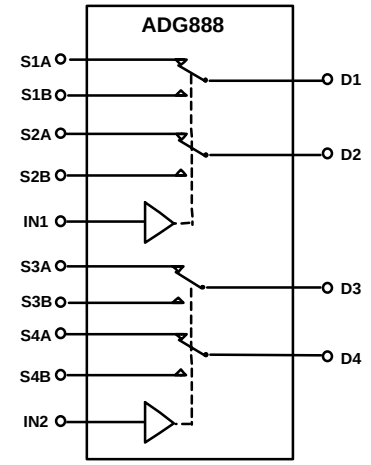
High current carrying capability:
- **400 mA continuous**
- **600 mA peak current at 5V**

Automotive temperature range: –40°C to +125°C
Rail-to-rail switching operation
Typical power consumption (<0.1 µW)

APPLICATIONS

Cellular phones
PDAs
MP3 players
Power routing
Battery-powered systems
PCMCIA cards
Modems
Audio and video signal routing
Communication systems

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

Figure 1.

GENERAL DESCRIPTION

The ADG888 is a low voltage Dual DPDT (double pole double throw) CMOS device. It has been optimized for high performance audio switching, and due to its low power and small physical size it is ideal for portable devices.

This device offers ultra-low on resistance of less than 0.8 Ω over the full temperature range, thus making the part an ideal solution for applications that require minimal distortion through the switch. The ADG888 also has the capability of carrying large amounts of current, typically 400mA at 5V operation.

The ADG888 is available in a 4 x 4 bump 2.0mm x 2.0mm WLCSP package, a 4mmx4mm 16 pin LFCSP package and a 16-lead TSSOP package. These packages make the ADG888 the ideal solution for space-constrained applications.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG888 exhibits break-before-make switching action.

PRODUCT HIGHLIGHTS

1. <0.8 Ω over full temperature range of –40°C to +125°C.

2. High current handling capability (400 mA continuous current at 5 V).

3. Low THD + N (0.02% typ).

4. Tiny 2 mm × 2 mm 16 ball WLCSP package, LFCSP and TSSOP package

Rev. PrD_02/05

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

ESD Caution 5
Pin Configurations 6
Terminology 6
Typical Performance Characteristics 7
Test Circuits 9
Outline Dimensions 11
Ordering Guide 12

REVISION HISTORY

SPECIFICATIONS[1]

Table 1. V_{DD} = 4.2V to 5.5V, GND = 0 V, unless otherwise noted

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.5			Ω typ	V_{DD} = 4.2 V, V_S = 0 V to V_{DD}, I_S = 100 mA;
	0.65	0.75	0.8	Ω max	Figure 7
On Resistance Match between	0.04			Ω typ	V_{DD} = 4.2 V, V_S = 2 V, I_S = 100 mA
Channels (ΔR_{ON})		0.075	0.08	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	0.1			Ω typ	V_{DD} = 4.2 V, V_S = 0 V to V_{DD},
		0.15	0.16	Ω max	I_S = 100 mA
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 0.6 V/4.5 V, V_D = 4.5 V/0.6 V; Figure 8
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 0.6 V or 4.5 V; Figure 9
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	25			ns typ	R_L = 50 Ω, C_L = 35 pF
	35	41	44	ns max	V_S = 3 V/0 V; Figure 10
t_{OFF}	16			ns typ	R_L = 50 Ω, C_L = 35 pF
	18	19	20	ns max	V_S = 3V/0V; Figure 10
BreakbeforeMake Time Delay (t_{BBM})	9			ns typ	R_L = 50 Ω, C_L = 35 pF
			5	ns min	V_{S1} = V_{S2} = 3 V; Figure 11
Charge Injection	200			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Figure 12
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 13
Channel-to-Channel Crosstalk	−90			dB typ	S1A−S2A/S1B−S2B;
					R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 16
	−67			dB typ	S1A−S1B/S2A−S2B;
					R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 15
Total Harmonic Distortion (THD + N)	0.02			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p
Insertion Loss	−0.05			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 14
−3 dB Bandwidth	25			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 14
C_S (OFF)	100			pF typ	
C_D, C_S (ON)	300			pF typ	
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.003			μA typ	Digital Inputs = 0 V or 5.5 V
		1	4	μA max	

[1]Temperature range is as follows: Y version: −40°C to +125°C.

[2]Guaranteed by design, not subject to production test.

SPECIFICATIONS[1]

Table 2. V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to VDD	V	
On Resistance (R_{ON})	0.7			Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD},
	0.95	1.0	1.1	Ω max	I_S = 100 mA; Figure 7
On Resistance Match between	0.04			Ω typ	V_{DD} = 2.7 V, V_S = 0.7 V,
Channels (ΔR_{ON})		0.08	0.085	Ω max	I_S = 100 mA
On Resistance Flatness ($R_{FLAT (ON)}$)	0.16			Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD},
		0.3	0.4	Ω max	I_S = 100 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 0.6 V/3.3 V, V_D = 3.3 V/0.6 V; Figure 8
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 0.6 V or 3.3 V; Figure 9
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.3	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	35			ns typ	R_L = 50 Ω, C_L = 35 pF
	50	58	63	ns max	V_S = 1.5 V/0 V; Figure 10
t_{OFF}	16			ns typ	R_L = 50 Ω, C_L = 35 pF
	20	21	22	ns max	V_S = 1.5 V/0V; Figure 10
Break-before-Make Time Delay (t_{BBM})	12			ns typ	R_L = 50 Ω, C_L = 35 pF
			5	ns min	V_{S1} = V_{S2} = 1.5 V; Figure 11
Charge Injection	135			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Figure 12
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 13
Channel-to-Channel Crosstalk	−90			dB typ	S1A−S2A/S1B−S2B;
					R_L = 50 V, C_L = 5 pF, f = 100 kHz;Figure 16
	−67			dB typ	S1A−S1B/S2A−S2B;
					R_L = 50 Ω, C_L = 5 pF, f = 100 kHz;Figure 14
Total Harmonic Distortion (THD + N)	0.022			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 1.5 V p-p
Insertion Loss	−0.06			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 14
−3 dB Bandwidth	57			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 14
C_S (OFF)	100			pF typ	
C_D, C_S (ON)	7300			pF typ	
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.003			μA typ	Digital Inputs = 0 V or 3.6 V
		1	4	μA max	

[1]Temperature range is as follows: Y version: −40°C to +125°C.
[2]Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS[1]

Table 3. T_A = 25°C, unless otherwise noted

Parameter	Rating
V_{DD} to GND	−0.3 V to +6 V
Analog Inputs[2]	−0.3 V to V_{DD} + 0.3 V
Digital Inputs[2]	−0.3 V to 6 V or 10 mA, Whichever Occurs First
Peak Current, S or D	600 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Continuous Current, S or D	400 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-lead TSSOP package	
θ_{JA} Thermal Impedance (4 layer board)	112°C/W
θ_{JC} Thermal Impedance	27.6°C/W
16 WLCSP Package	
θ_{JA} Thermal Impedance (4 layer board)	130°C/W
16 LFCSP Package	
θ_{JA} Thermal Impedance (4 layer board)	30.4 °C/W
IR Reflow, Peak Temperature <20 sec	235°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2] Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

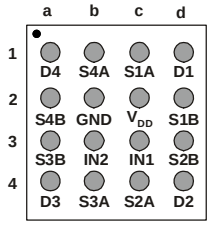
Table 4. ADG888 Truth Table

Logic (IN1/IN2)	Switch 1A/2A/3A/4A	Switch 1B/2B/3B/4B
0	Off	On
1	On	Off

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS



TOP VIEW
(Solder Bumps on opposite side)

Figure 2. 16-Lead WLCSP (CB-16)

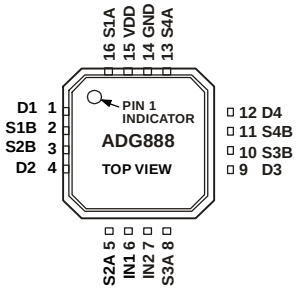


Figure 3. 16-Lead LFCSP (CP-16)

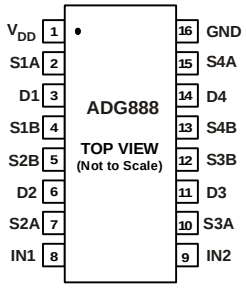


Figure 4. 16-Lead TSSOP (RU-16)

TERMINOLOGY

V_{DD}	Most positive power supply potential.
I_{DD}	Positive supply current.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
V_D (V_S)	Analog voltage on terminals D, S.
R_{ON}	Ohmic resistance between D and S.
$R_{FLAT (ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured
ΔR_{ON}	On resistance match between any two channels.
I_S (OFF)	Source leakage current with the switch off.
I_D (OFF)	Drain leakage current with the switch off.
I_D, I_S (ON)	Channel leakage current with the switch on.
V_{INL}	Maximum input voltage for Logic 0.
V_{INH}	Minimum input voltage for Logic 1.
I_{INL} (I_{INH})	Input current of the digital input.
C_S (OFF)	Off switch source capacitance. Measured with reference to ground.
C_D (OFF)	Off switch drain capacitance. Measured with reference to ground.
C_D, C_S (ON)	On switch capacitance. Measured with reference to ground.
C_{IN}	Digital input capacitance.
t_{ON}	Delay time between the 50% and the 90% points of the digital input and switch on condition.
t_{OFF}	Delay time between the 50% and the 90% points of the digital input and switch off condition.
t_{BBM}	On or off time measured between the 80% points of both switches when switching from one to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.
Off Isolation	A measure of unwanted signal coupling through an off switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
−3 dB Bandwidth	The frequency at which the output is attenuated by 3 dB.
On Response	The frequency response of the on switch.
Insertion Loss	The loss due to the on resistance of the switch.
THD + N	The ratio of the harmonic amplitudes plus noise of a signal, to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

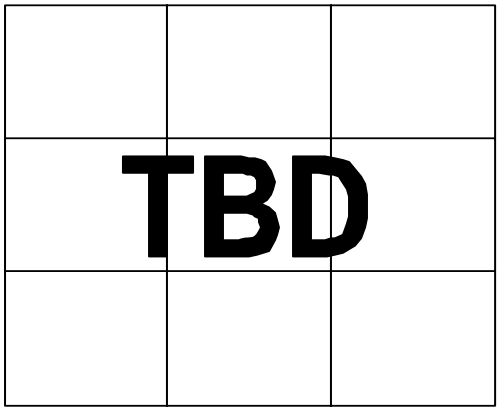


Figure 4. On Resistance vs. V_D (V_S) V_{DD} = 4.2V to 5.5V

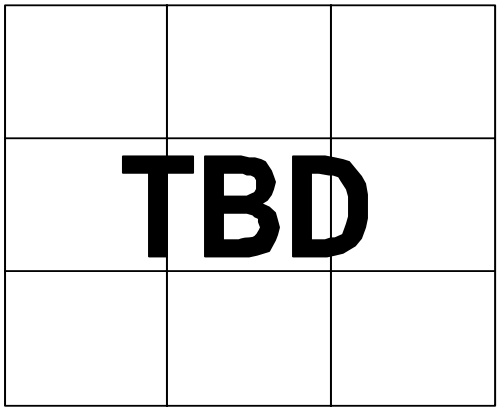


Figure 5. On Resistance vs. V_D (V_S) V_{DD} = 2.7 V to 3.6 V

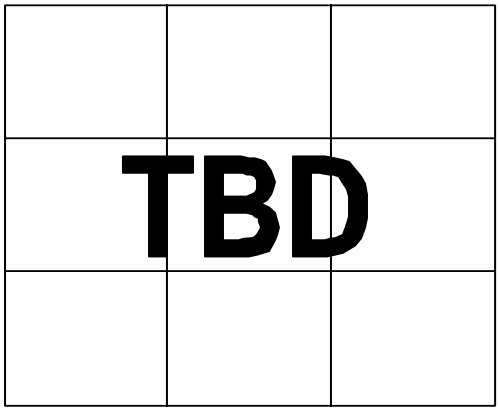


Figure 6. On Resistance vs. V_D (V_S) for Different Temperature, 5.5 V

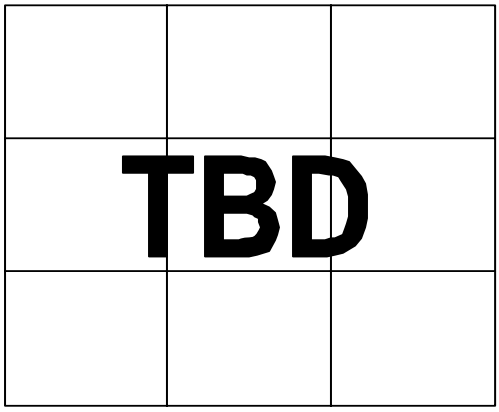


Figure 7. On Resistance vs. V_D (V_S) for Different Temperature, 3.3V

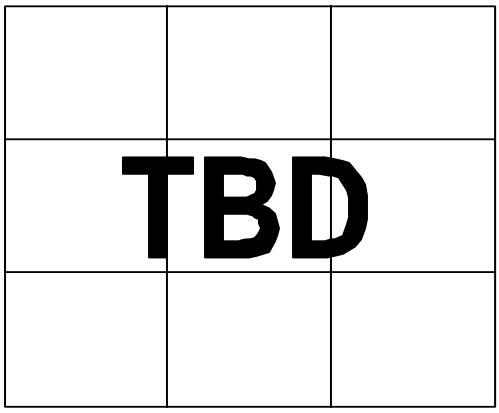


Figure 8. Leakage Current vs. Temperature, 5.5 V

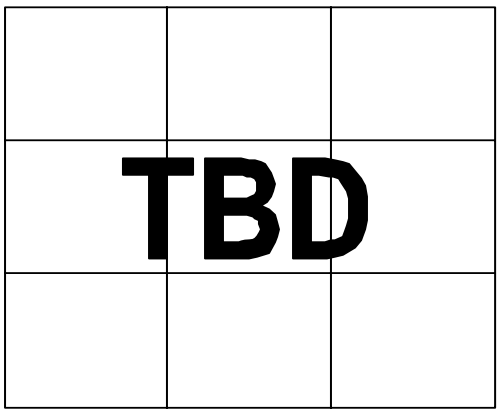


Figure 9. Leakage Current vs. Temperature, 4.2 V

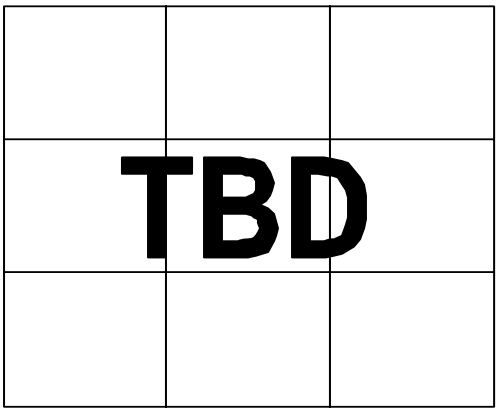


Figure 9. Leakage Current vs. Temperature, 3.3 V

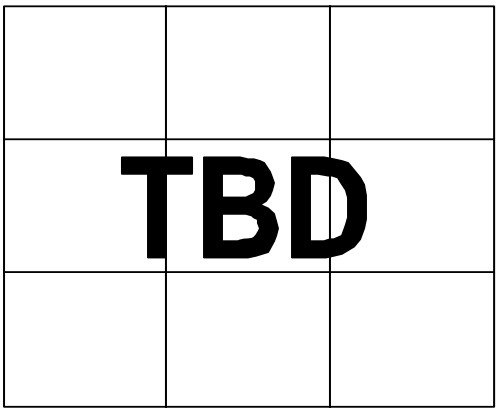


Figure12. Bandwidth

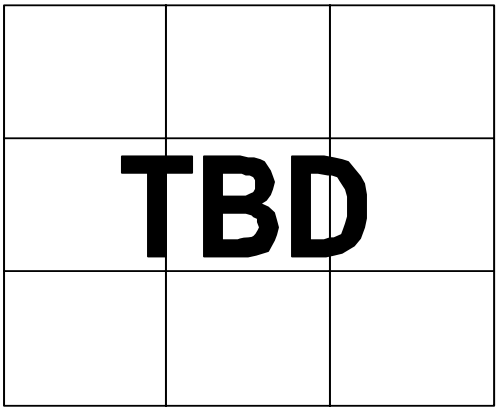


Figure 6. Charge Injection vs. Source Voltage

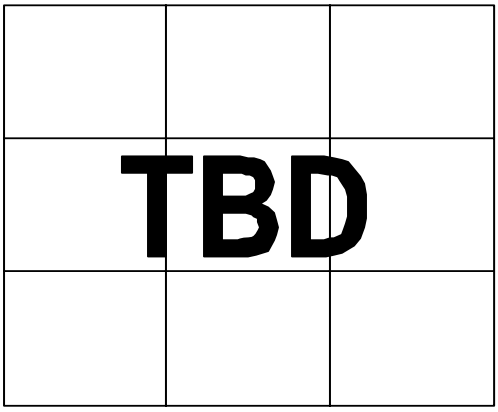


Figure14. Off Isolation vs. Frequency

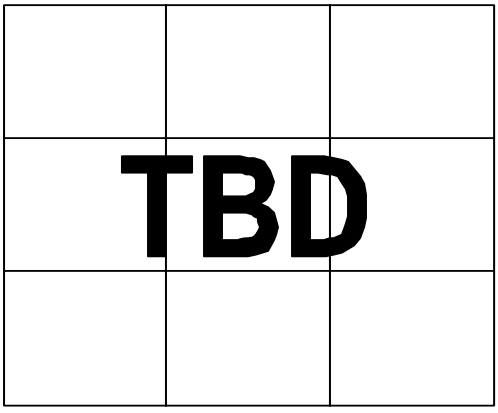


Figure 11. t_{ON}/t_{OFF} Times vs. Temperature

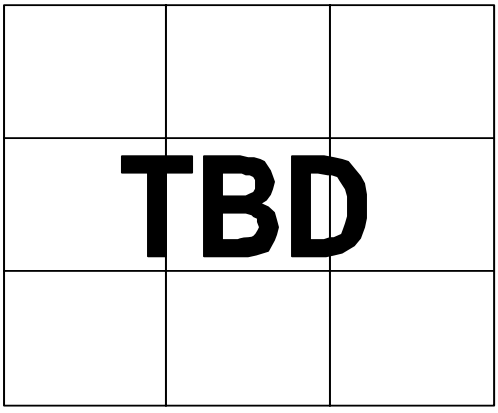


Figure 15. Crosstalk vs. Frequency

TEST CIRCUITS

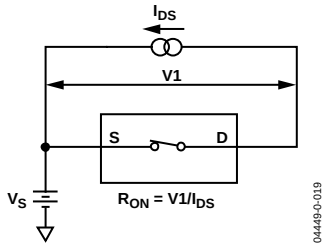


Figure 7. On Resistance

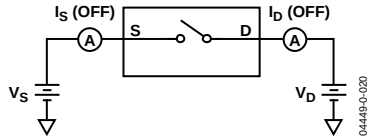


Figure 8. Off Leakage

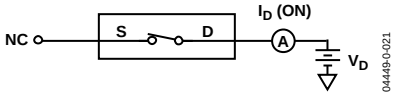


Figure 9. On Leakage

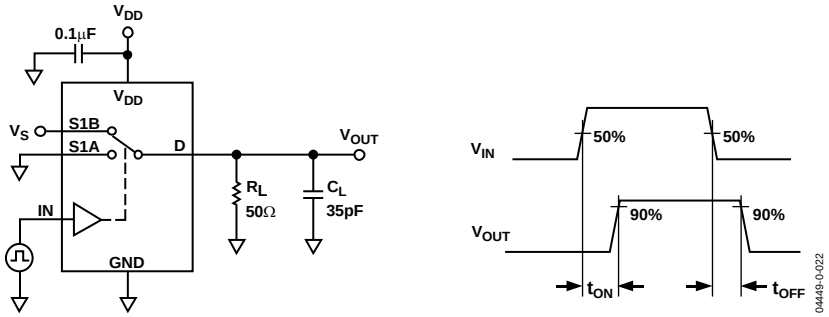


Figure 10. Switching Times, t_{ON}, t_{OFF}

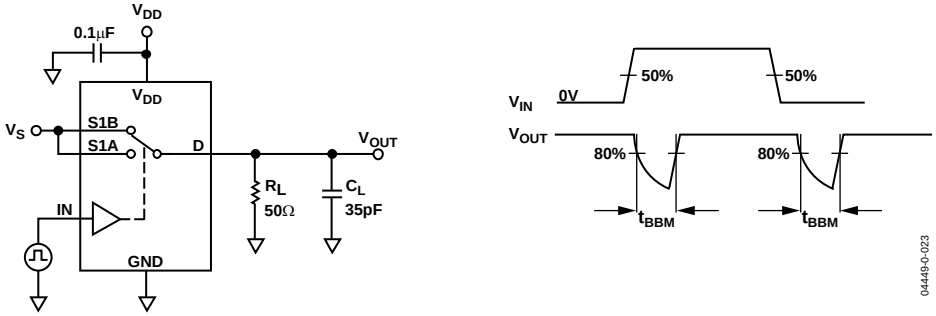


Figure 11. Break-before-Make Time Delay, t_{BBM}

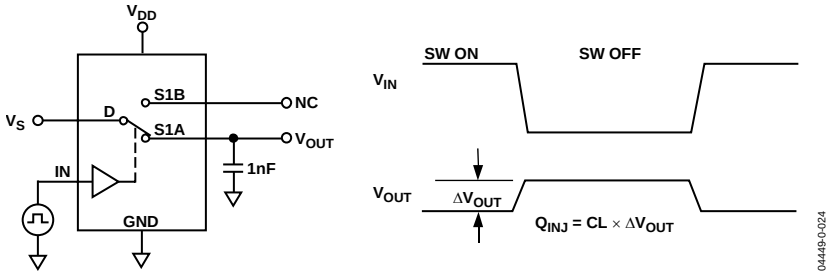
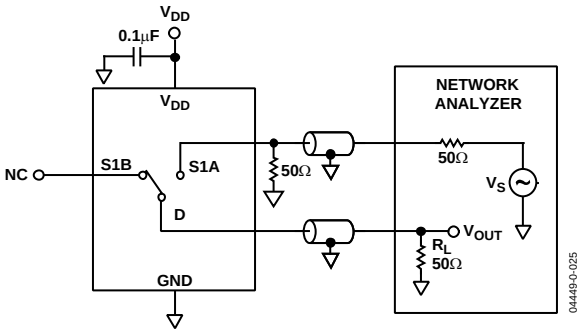
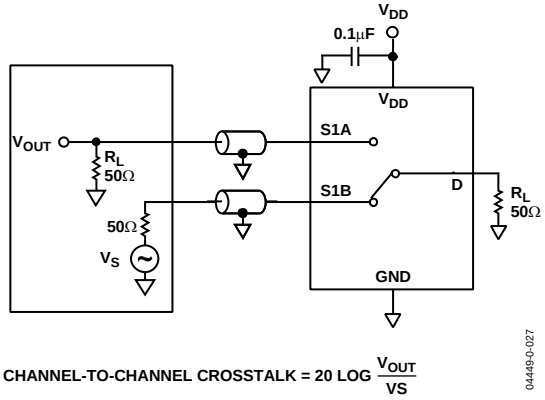


Figure 12. Charge Injection



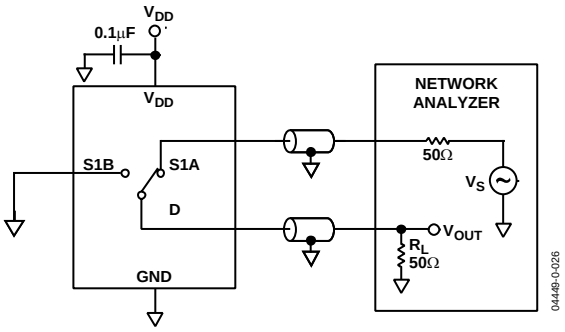
$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{VS}$$

Figure 13. Off Isolation



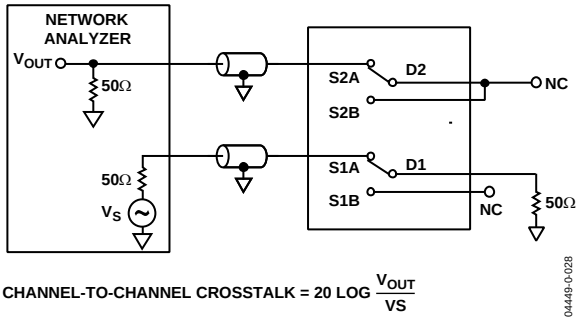
$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{VS}$$

Figure 14. Channel-to-Channel Crosstalk (S1A–S1B)



$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}}$$

Figure 15. Bandwidth



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{VS}$$

Figure 16. Channel-to-Channel Crosstalk (S1A–S2A)

OUTLINE DIMENSIONS

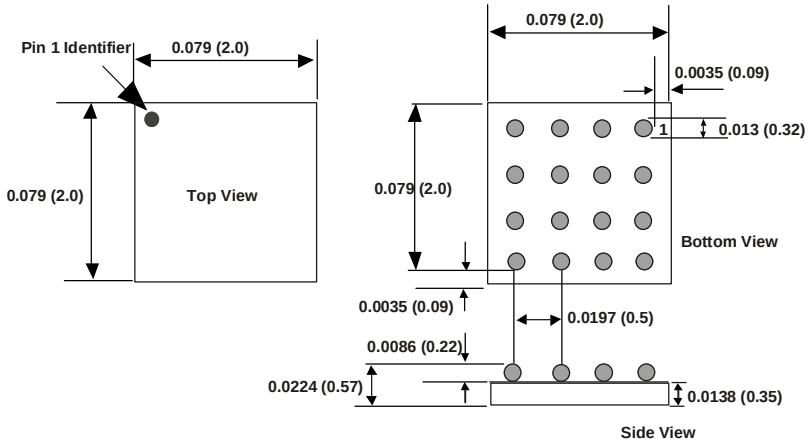


Figure 177. Outline Dimension [WLCSP] (CB-16)
Dimensions shown in inches (millimeters)

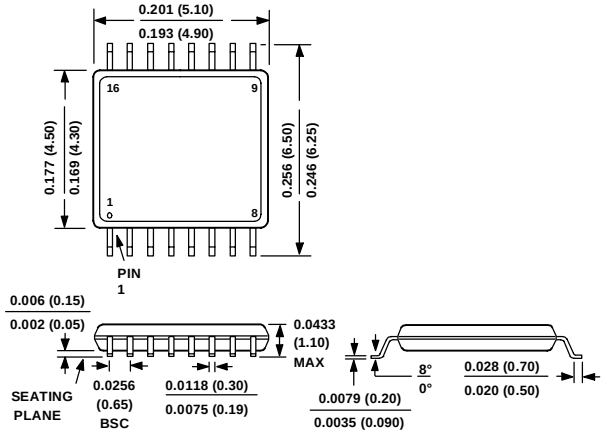


Figure 18. Outline Dimension [TSSOP] (RU-16)
Dimensions shown in millimeters

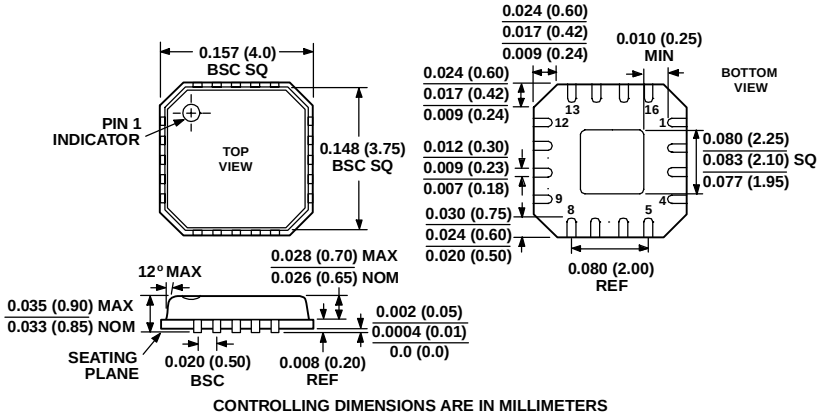


Figure 19. Outline Dimension [LFCSP] (CP-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG888YRU	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG888YCP	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP)	CP-16	
ADG888YCB	-40°C to +125°C	Micro Chip Scale Package (WLCSP)	CB-16	S0D

[1]Branding on this package is limited to three characters due to space constraints

PR05432-0-7/05(PrD)